WHAT IS CLAIMED IS:

1. A method of encoding a sequence of information bits in a communication system comprising:

dividing said sequence of information bits into encoding bits and parallel bits;

encoding said encoding bits to produce encoded bits;

mapping said encoded bits and said parallel bits into first and second pulse amplitude modulation (PAM) signals; and

generating a quaternary amplitude modulation (QAM) signal from said first and said second PAM signals.

2. The method of claim 1, further comprising:

transmitting said QAM signal from said communication system associated with said method of encoding.

3. The method of claim 2, wherein said communication system is an asymmetric digital subscriber line (ADSL) communication system.

4. The method of claim 1, further comprising:

identifying whether a number of said information bits is odd or even.

5. The method of claim 4, further comprising:

selecting a mode of operation based on an odd or even status of said number of said information bits.

6. The method of claim 5, wherein said mode of operation determines a number of said encoding bits, a puncture pattern used in said encoding, a coding rate used in said encoding, and a number of said encoded bits and said parallel bits used in said mapping.

7. The method of claim 5, wherein said selecting is made between a first mode of operation and a second mode of operation.

8. The method of claim 4, wherein if a number of said information bits is even, a number of said encoding bits is two.

9. The method of claim 4, wherein if a number of said information bits is even, a number of said coding bits is greater than two.

10. The method of claim 4, wherein if a number of said information bits is odd, a number of said encoding bits is three.

11. The method of claim 4, wherein if a number of said information bits is odd, a number of said coding bits is greater than three.

12. The method of claim 1, wherein said encoded bits consist of systematic bits and parity bits.

13. The method of claim 12, wherein if a number of said information bits is even, a number of said systematic bits is two and a number of said parity bits is two.

14. The method of claim 12, wherein if a number of said information bits is odd, a number of said systematic bits is three and a number of said parity bits is one.

15. The method of claim 1, wherein said encoding is performed by a turbo encoder.

16. The method of claim 1, wherein said encoding is performed by multiple turbo encoders.

17. The method of claim 1, wherein said encoding is performed by a serial concatenated turbo encoder.

18. The method of claim 1, wherein said encoding is performed by a turbo product code encoder.

19. The method of claim 1, wherein said encoding is performed by an low density parity check (LDPC) encoder.

20. The method of claim 1, wherein said mapping includes:

forming a first vector and a second vector from said encoded bits and said parallel bits.

21. The method of claim 20, wherein said mapping further includes:

mapping said first vector to said first PAM signal and mapping said second vector to said second PAM signal.

22. The method of claim 20, wherein each of said first and said second vectors is formed from alternate ones of said encoded bits and said parallel bits.

23. The method of claim 22, wherein said alternate ones of said encoded bits form least significant bits and said alternate ones of said parallel bits form most significant bits of each of said first and said second vectors.

24. The method of claim 1, wherein said mapping is a concatenated Gray mapping.

25. The method of claim 24, wherein said concatenated Gray mapping is a serial concatenation of an inner Gray mapping and an outer Gray mapping.

26. The method of claim 26, wherein said inner Gray mapping is applied to said encoded bits and said outer Gray mapping is applied to said parallel bits.

27. An apparatus for encoding a sequence of bits in an asymmetric digital subscriber line (ADSL) system, comprising:

a plurality of signal lines configured to divide said sequence of information bits into encoding bits and parallel bits;

at least one turbo encoder configured to encode said encoding bits to produce encoded bits; and

a quaternary amplitude modulation (QAM) unit configured to map said encoded bits and said parallel bits into first and second pulse amplitude modulation (PAM) signals and to generate a QAM signal from said first and said second PAM signals.

28. The apparatus of claim 27, further comprising:

a control unit configured to identify whether a number of said information bits is odd or even.

29. The apparatus of claim 28, wherein said control unit is further configured to generate a mode control signal based on an odd or even status of said number of information bits.

30. The apparatus of claim 29, wherein said mode control signal is provided to said at least one turbo encoder and said QAM unit to determine a number of said encoding bits, a puncture pattern used in said encoding, a coding rate used in said encoding, and a number of said encoded bits and said parallel bits used in said mapping.

31. The apparatus of claim 28, wherein if a number of said information bits is even, a number of said encoding bits is two.

32. The apparatus of claim 28, wherein if a number of said information bits is even, a number of said coding bits is greater than two.

33. The apparatus of claim 28, wherein if a number of said information bits is odd, a number of said encoding bits is three.

34. The apparatus of claim 28, wherein if a number of said information bits is odd, a number of said coding bits is greater than three.

35. The apparatus of claim 27, wherein said encoded bits consist of systematic bits and parity bits.

36. The apparatus of claim 35, wherein if a number of said information bits is even, a number of said systematic bits is two and a number of said parity bits is two.

37. The apparatus of claim 35, wherein if a number of said information bits is odd, a number of said systematic bits is three and a number of said parity bits is one.

38. The apparatus of claim 27, wherein said at least one turbo encoder comprises multiple turbo encoders.

39. The apparatus of claim 27, wherein said at least one turbo encoder comprises at least one serial concatenated turbo encoder.

40. The apparatus of claim 27, wherein said at least one turbo encoder comprises at least one turbo product code encoder.

41. The apparatus of claim 27, wherein said at least one turbo encoder comprises a low density parity check (LDPC) encoder.

42. The apparatus of claim 27, wherein said QAM unit is further configured to form a first vector and a second vector from said encoded bits and said parallel bits.

43. The apparatus of claim 42, wherein said QAM unit is further configured to map said first vector to said first PAM signal and mapping said second vector to said second PAM signal.

44. The apparatus of claim 42, wherein said QAM unit is further configured to form each of said first and said second vectors from alternate ones of said encoded bits and said parallel bits.

45. The apparatus of claim 44, wherein said QAM unit is further configured to use said alternate ones of said encoded bits to form least significant bits and said alternate ones of said parallel bits to form most significant bits of each of said first and said second vectors.

46. The apparatus of claim 27, wherein said QAM unit is further configured to use a concatenated Gray mapping to map said encoded bits and said parallel bits.

47. The apparatus of claim 46, wherein said QAM unit is further configured to implement said concatenated Gray mapping as a serial concatenation of an inner Gray mapping and an outer Gray mapping.

48. The apparatus of claim 47, wherein said QAM unit is further configured to apply said inner Gray mapping to said encoded bits and said outer Gray mapping to said parallel bits.